REMARKS

The claims are claims 1 to 12.

Claims 4, 6 and 12 are amended in response to the rejections under 35 U.S.C. 112.

The FINAL REJECTION objects to previous drawing change. The FINAL REJECTION states that "there is no evidence in the original disclosure to support the removing of arrows from the lines in Figure 4." The FINAL REJECTION further states there appears no input to merge 46.

The Applicant respectfully submits that this is incorrect. The original application states at page 6, lines 10 and 11:

> "Figure 4 illustrates an electrical connection view of the coupling between the access adapter and the target system;"

The original application also states at page 11, lines 3 and 4:

> "Figure 4 illustrates an electrical connection view of the coupling between access adapter 2 and target system 3."

The Applicant respectfully submits that it is known in the art that display line arrows are not customarily used on electrical connection diagrams to show signal flow. Thus the original application does provide support for removing the arrows in Figure 4. Since the electrical connection s of Figure 4 do not show signal flow, there is no lack of showing the input to merge 46.

The FINAL REJECTION objects to the prior amendment for introducing new matter. The FINAL REJECTION notes the addition of "said start bit generator generating a serial signal having a predetermined number of bits" and "data stored in said alternative data output register" to claim 12 in paper number 10.

The recitation "said start bit generator generating a serial signal having a predetermined number of bits" has been deleted from claim 12. The recitation "data stored in said alternative data output register" in claim 12 has been changed to "a predetermined number of bits of output data stored in said alternative data output register." This amended recitation corresponds to the recitation "output switch 202 then selects data register OUT 212 for serial transmission of the predetermined number of bits" of page 19, lines 25 to 27 of the application. Accordingly, amended claim 12 does not include new matter.

The patent number of amended page 1, lines 16 and 17 has been corrected to correspond to the provisional application number and the patent application serial number. The prior amendment inadvertently mixed the numbers and title of the paragraphs at page 1, line 14 and 15 and page, 1, lines 16 and 17.

Claim 6 was objected to as informal because lines 5 and 6 recited "a start bit detector having a start bit detector input input." Amended claim 6 deletes one of these recitations of "input."

Claims 4 and 6 to 12 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The FINAL REJECTION cites the following improper limitations: claim 4, line 8 "a predetermined number"; claim 6, line 11 "a first predetermined number"; and claim 12, line 7 "a predetermined number."

Claims 4, 6 and 12 have been amended in response to this rejection. The recitation of "a predetermined number of bits" at lines 8 and 9 of claim 4 has been canceled. Claim 6 has been amended to delete recitation of "greater than a first predetermined

number." Claim 12 has been amended to delete recitation of "generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first digital state." By these deletions, claims 4, 6 and 12 no longer recite subject matter not taught in the application as originally filed. Accordingly, this rejection should be withdrawn.

This rejection further cites lines 10, 13 and 14 of claim 12 as reciting subject matter not originally described. The FINAL REJECTION argues that the original application teaches output switch 202 connects for output only "the predetermined number of bits" stored in register OUT 212 and not the "data stored in said alternative data output register" as currently recited in claim 12. Claim 12 has been amended to recite that the start bit generator generates "a predetermined number of bits of output data stored in said alternative data output register." The recitation of the output switch has been similarly amended to recite connecting "said predetermined number of bits of output data stored in said alternative data output register to said test data output." The Applicant respectfully submits that these recitations are fully described in the application as originally filed.

Claims 1 to 12 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The FINAL REJECTION states that the original recitation at page 18, lines 19 and 20 of "This data transfer protocol includes a first section 121 of plural bits of the same digital state," fails to disclose how to determine those plural bits.

The Applicant respectfully submits that the original disclosure does teach how to determine this number of bits without undue experimentation. Claim 1 originally recited at lines 8 to 12

"supplying to the test access port for communication to the boundary-scan architecture a serial signal having a first logic state for a number of cycles greater in number than a number of bits of the serial connection of the plurality of registers." The original ABSTRACT recited at lines 6 to 9 "The external emulation hardware supplys a serial signal having a first logic state for a number of cycles greater in number than a number of bits of the serial connection of registers to the test access port." The number of bits of the serial connection of the plurality of registers results from the product design and is presumably known to anyone who would construct a product using this invention. With the dimensions of the serial chain of shift registers presumably known, this predetermined number of bits is easily determined. Thus undue experimentation is not required. Accordingly, this rejection should be withdrawn.

Claims 6 to 12 were rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. The FINAL REJECTION states that claim 6 omits the essential step of being a selected module because any nonselected module will be nonresponsive to data on the serial connection.

Claim 6 does not omit an essential step or element of this invention. Claim 6 recites that the input switch and the output switch route data through the serial scan path in a serial scan path mode and route data through the start bit detector in an alternative data transfer protocol mode. This module is made insensitive to the serial scan data in the serial scan path mode. Note in the serial scan path mode the input data does not reach the start bit detector and thus the module does not respond to this data. It is clear to one skilled in the art that this nonresponsiveness does not prevent the module from passing the data

along the serial chain as recited in claim 6 in the serial scan path mode. Accordingly, this rejection should be withdrawn.

Claims 4 and 6 to 12 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The FINAL REJECTION states that the limitation "said predetermined number of data bits" in line 12 of claim 4 is vague and indefinite because "a predetermined number of data bits" has been recited both in lines 18 and 19 of claim 1 and in lines 5 and 6 of claim 4. This limitation in claim 4 has been changed to "said identified predetermined number of data bits to be transmitted." This change makes clear that this refers to the recitation earlier in this paragraph of claim 4.

The FINAL REJECTION states that the limitations "said serial data input" and "said serial data output" in, for example, lines 23 and 29 of claim 6 have insufficient antecedent basis for these limitations in the claim. Claim 6 has been amended to change "said serial data input" to "said serial input" and to change "said serial data output" to "said serial output." These limitations have antecedent basis in line 2 of claim 6.

The FINAL REJECTION states that the limitation "said mode input" in lines 31 and 34 of claim 6 and at claim 8, line 10 is vague and indefinite because "a mode input" recited in lines 21 and 22 of the claim is associated with input switch. Claim 6 has been amended at line 28 to state that the output switch also includes a mode input. This mode input to the output switch is described in the original application at page 19, lines 3 and 4 and illustrated in Figure 8. This recitation provides proper antecedent basis for the late limitation in claims 6 and 8.

The FINAL REJECTION states at page 7, paragraph 11 that Claims 1 to 12 are deemed non-obvious over the prior art of record, and

would be allowed once the above rejections under 35 U.S.C. 112, first and second paragraphs are overcome. The Applicant respectfully submits that the preceding amendments and remarks are fully responsive to the rejections under 35 U.S.C. 112. Accordingly, claims 1 to 12 should be allowed.

The Applicant respectfully requests entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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